



# atomera

Investor Presentation  
September 2018

**NASDAQ: ATOM**

# Note Regarding Forward-Looking Statements



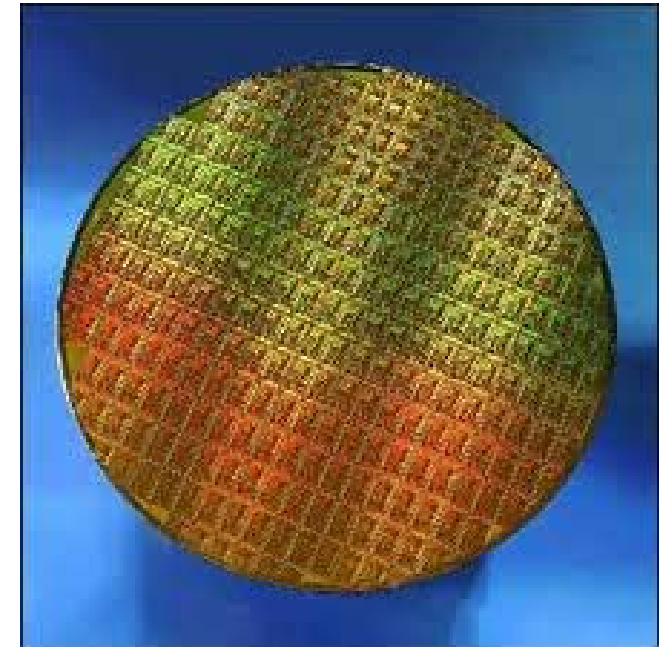
This presentation contains forward-looking statements concerning Atomera Incorporated (“Atomera,” the “Company,” “we,” “us,” and “our”). The words “believe,” “may,” “will,” “potentially,” “estimate,” “continue,” “anticipate,” “intend,” “could,” “would,” “project,” “plan,” “expect” and similar expressions that convey uncertainty of future events or outcomes are intended to identify forward-looking statements. These forward-looking statements are subject to a number of risks, uncertainties and assumptions, including those described in the “Risk Factors” section of our Annual Report on Form 10-K for the year ended December 31, 2017 filed with the SEC on March 6, 2018 (the “2017 Annual Report”). In light of these risks, uncertainties and assumptions, the forward-looking events and circumstances discussed in this presentation may not occur and actual results could differ materially and adversely from those anticipated or implied in our forward-looking statements. You should not rely upon forward-looking statements as predictions of future events. Although we believe that the expectations reflected in our forward-looking statements are reasonable, we cannot guarantee that the future results, levels of activity, performance or events and circumstances described in the forward-looking statements will be achieved or occur.

This presentation contains only basic information concerning Atomera. The Company’s filings with the Securities Exchange Commission, including the 2017 Annual Report, include more information about factors that could affect the Company’s operating and financial results. We assume no obligation to update information contained in this presentation. Although this presentation may remain available on the Company’s website or elsewhere, its continued availability does not indicate that we are reaffirming or confirming any of the information contained herein.

# Investment Overview



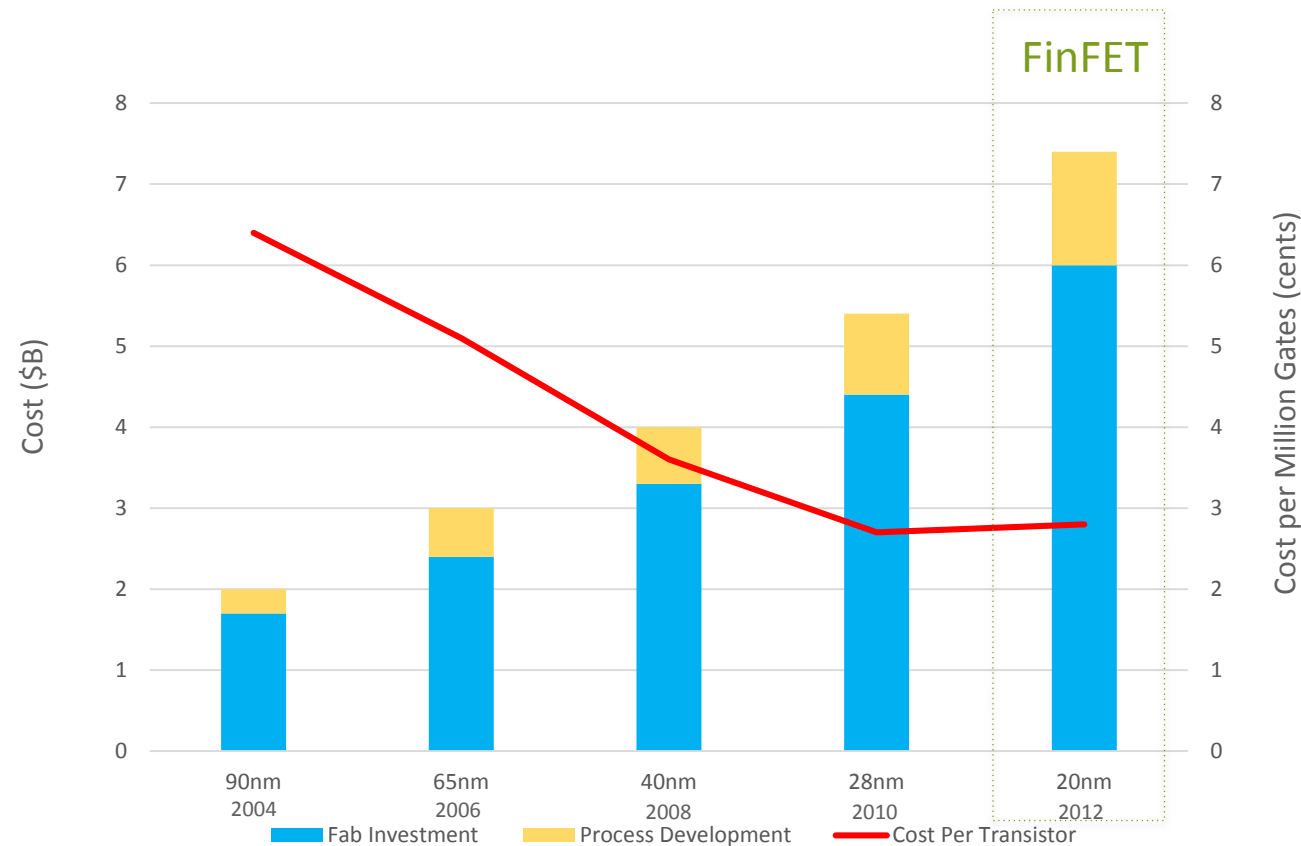
- Mears Silicon Technology (MST®) is a semiconductor enhancement technology
  - Improves electron mobility resulting in higher performance, lower power, and lower costs
- Capital-light IP licensing business
  - Highly leverageable business model with strong cash position
  - Robust and growing patent portfolio to support licensing activities
- Currently engaged with 50% of world's top semiconductor makers
  - Total available market: \$4.0 B
- Strong team to commercialize technology
  - CEO ran \$1B+ divisions at Broadcom and Altera
  - Founder/CTO co-invented the erbium-doped fiber amplifier
- NASDAQ Ticker: "ATOM" – IPO in August 2016



# Extending Moore's Law



## The skyrocketing cost of new nodes



Source: McKinsey & Co, "On Semiconductors"

## MST: A way out

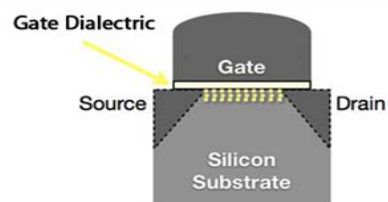
- MST can deliver a half to a full node of benefits
  - Extends life of depreciated fabs
  - Continues reducing the cost per transistor
  - May solve problems in geometries smaller than 28 nm
- MST cost is tiny in comparison to developing a new node
  - Process development/licensing is ~\$10M
  - Foundry equipment upgrades cost is ~\$30-50M
  - A foundry for a new node costs billions

**"From an economic standpoint, Moore's law is over."**

Silicon Valley analyst Lynley Gwynnap, quoted in "After Moore's Law," *The Economist*, 12 March 2016

# MST Technology

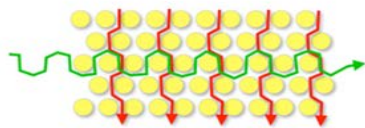
## STANDARD SILICON TRANSISTOR



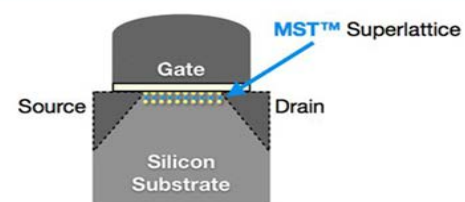
Standard Silicon  
Atomic Structure



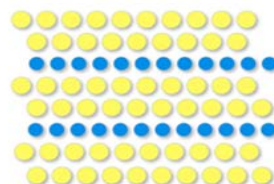
LIMITED Horizontal Current Flow +  
EXCESSIVE Vertical Leakage



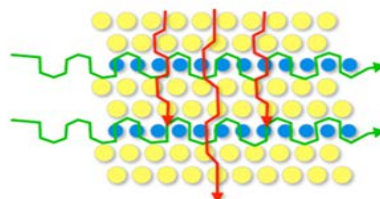
## MST SILICON TRANSISTOR



MST™ Silicon  
Atomic Structure



INCREASED Horizontal Current Flow +  
REDUCED Vertical Leakage



## Potential Benefits

- Improved Efficiency
  - Improved performance
  - Lower power consumption
  - Some combination of the two
- Reduced Die Size
  - Lower power needs
  - Lower bottom line cost
- Improved Yield
  - Less waste
  - Easier design parameters

# Semiconductor Ecosystem



Process  
Development

Wafer Fabrication

Chip Makers / Sellers

Equipment  
Manufacturers

Foundries



GLOBALFOUNDRIES®

UMC

Integrated Device Manufacturers (IDM)



TEXAS INSTRUMENTS



Fabless



Vertically Integrated Firms



Microsoft

Supporting Ecosystem

Semiconductor Equipment Manufacturers



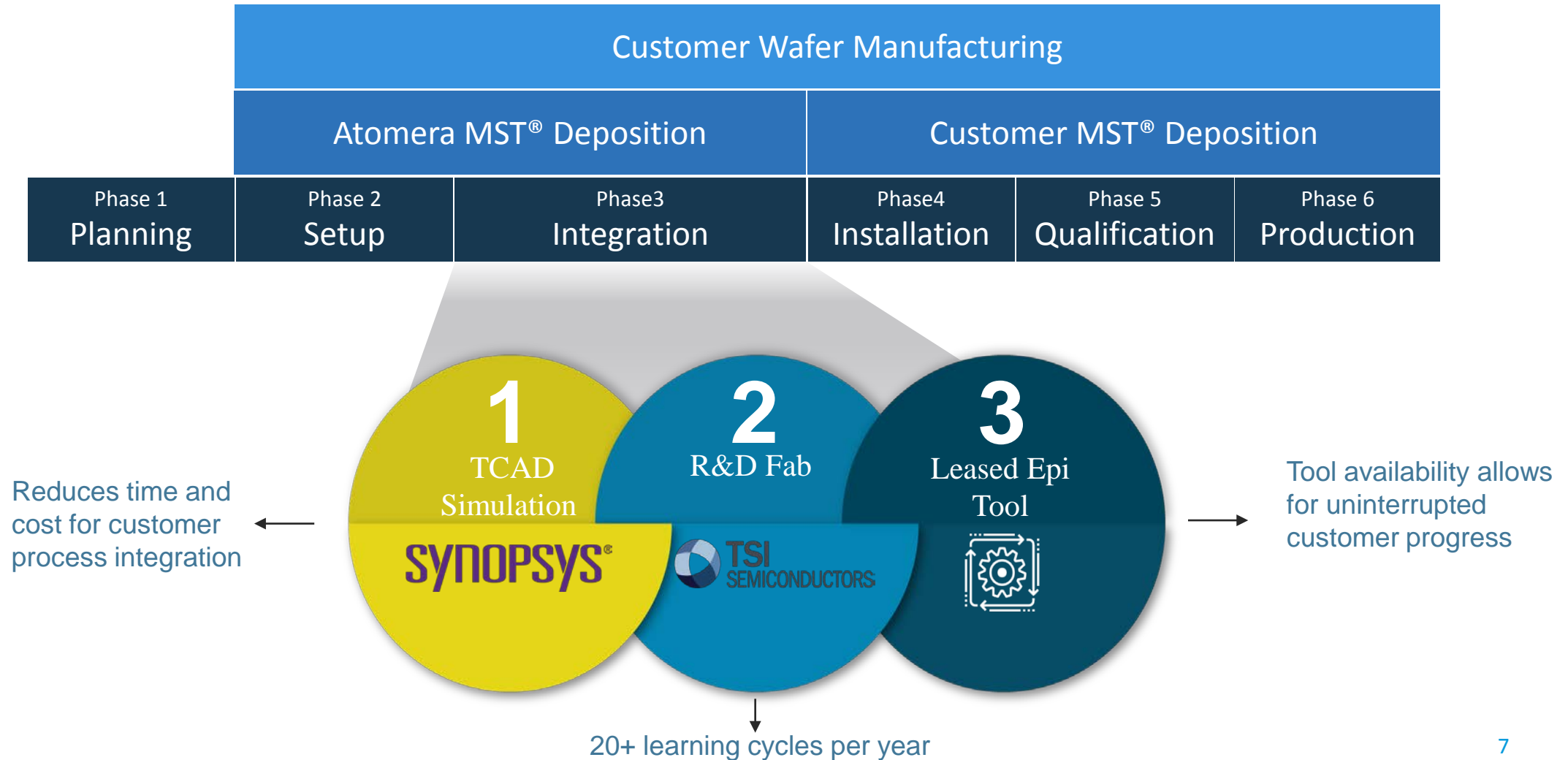
HITACHI

Electronic Design Automation Tools

synopsys®

cadence

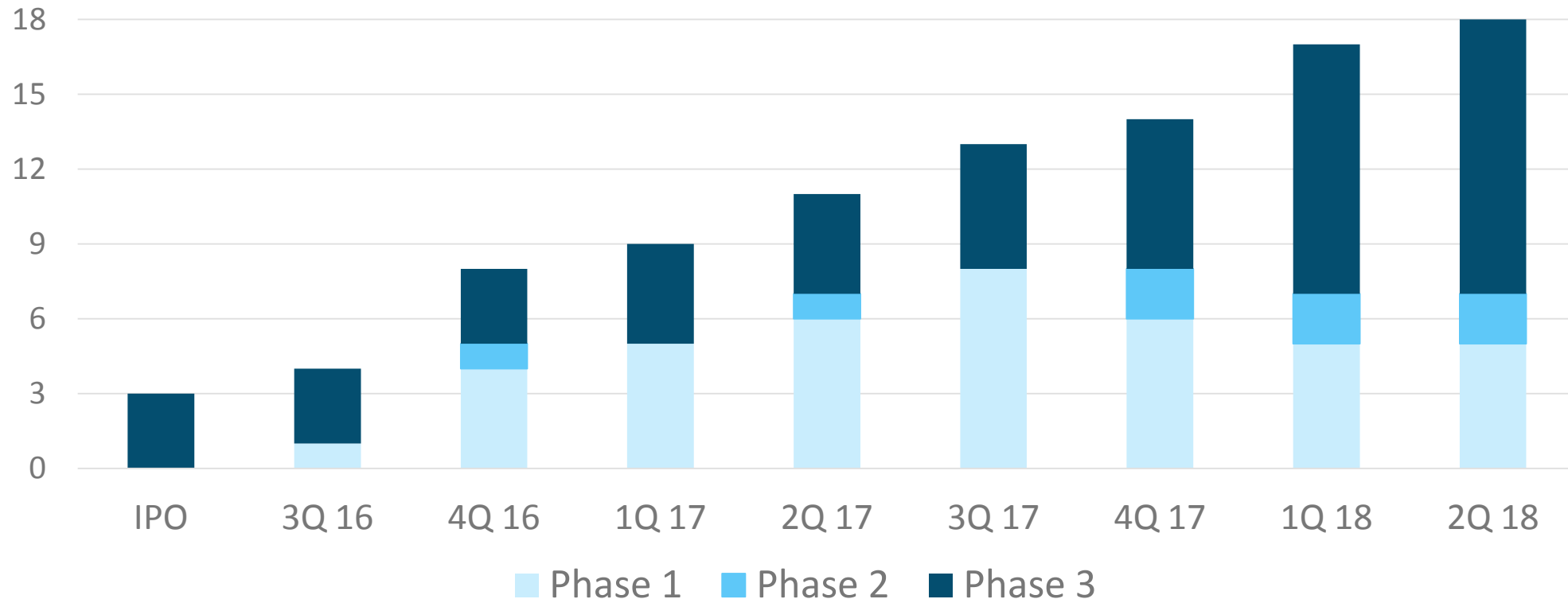
# Accelerating time to license



# Customer Engagement Pipeline



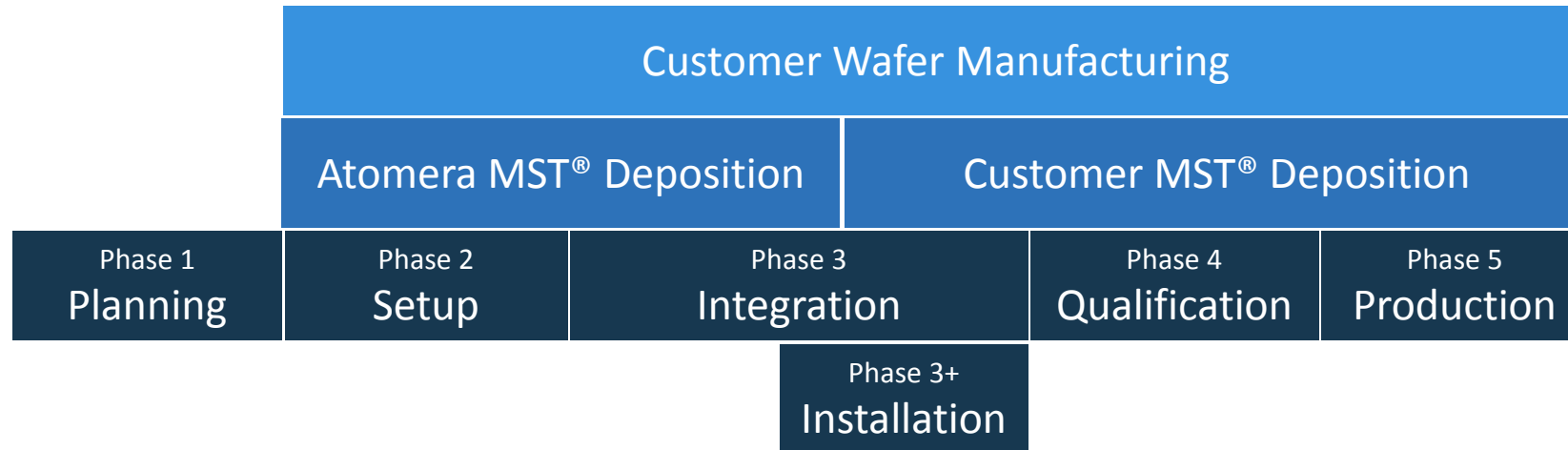
## Number of Customer Engagements



- 14 customers, 18 engagements
- Now engaged with 50% of the world's top semiconductor makers\*
- \* 10 of the top 20 (IC Insights, McClean Report 2017)



# Early Installation Advantages



- Significantly lowers cost of processing test wafers
- Speeds throughput by avoiding shipping/contamination/calibration time
- Improves capacity – both for Epi tools and our engineers
- Raises our stature within Epi OEMs
- Customer Epi engineers become an internal advocate for multiple process nodes

# Largest Companies with fabs

	Company	Type	Market Segment	Total Capacity - Wf/mon. (200mm equ)
1	Samsung Semiconductor	IDM	Memory	2,598,750
2	TSMC	Foundry	Logic	2,012,317
3	Micron Technology	IDM	Memory	1,540,500
4	SK Hynix	Foundry	Memory	1,530,000
5	Toshiba Semiconductor	IDM	Memory	1,158,750
6	GlobalFoundries	Foundry	Logic	810,000
7	Intel	IDM	MCU	681,750
8	Texas Instruments (TI)	IDM	Analog	620,879
9	UMC (United Microelectronics)	Foundry	Logic	614,863
10	STMicroelectronics	IDM	Analog	461,006
11	SMIC	Foundry	Logic	432,750
12	Infineon Technologies	IDM	Analog	375,809
13	ON Semiconductor	IDM	Analog	374,492
14	Powerchip Technology	Foundry	Logic	313,000
15	TowerJazz	Foundry	Analog	297,735
16	NXP Semiconductors	IDM	Analog	250,000
17	Renesas Electronics	IDM	Other	236,124
18	Japan Semiconductor Corp. (Toshiba)	Foundry	Analog	229,944
19	Huahong Grace Semiconductor (HHGrace)	Foundry	Analog	213,000
20	IM Flash	IDM	Memory	180,000
21	Vanguard International Semiconductor (VIS)	Foundry	Analog	175,000
22	MagnaChip Semiconductor	Foundry	Analog	155,000
23	Nanya Technology	IDM	Memory	135,000
24	Fujitsu Semiconductor	IDM	Logic	131,728
25	China Resources Microelectronics (CR Micro)	IDM	Analog	130,846

- Total industry capacity 17.8M wafers/month
- Top 25 wafer capacity leaders
  - 89% of total industry capacity at end of 2016

# Atomera Business Opportunity



## License Fees

## Engineering Service Fees

### Royalties

Example 1. Worldwide Average Fab <sup>1</sup>		Example 2. Leading Foundry, 40nm Fab	
Monthly Fab Capacity (wafers/month)	40,000	Monthly Fab Capacity (wafers/month)	80,000
Wafer ASP	\$1,637	Wafer ASP	\$3,000
<b><i>Annual Revenue Potential<sup>2</sup></i></b>	<b><i>\$7.9M</i></b>	<b><i>Annual Revenue Potential<sup>2</sup></i></b>	<b><i>\$28.8M</i></b>

1. 2016: 375 fabs worldwide with a total of 15.2M wafers per month

2. Assumes 50% penetration

Sources: IC Insights

# Technology and Market Segment



IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 64, NO. 1, JANUARY 2017

329

Comparison of SOI Versus Bulk FinFET Technologies for 6T-SRAM Voltage Scaling at the 7-/8-nm Node



Punch-Through Stop Doping Profile Control via Interstitial Trapping by Oxygen-Insertion Silicon Channel



IEEE Electron Devices Society

2017

The Impact of Oxygen Insertion Technology on SRAM Yield Performance

**AIP** | Journal of Applied Physics

Effects of Oxygen-Inserted Layers on Diffusion of Boron, Phosphorus, and Arsenic in Silicon for Ultra-Shallow Junction Formation

**Leading Analog**

**Mainstream**

**Planar Extension**

**Advanced 3D**

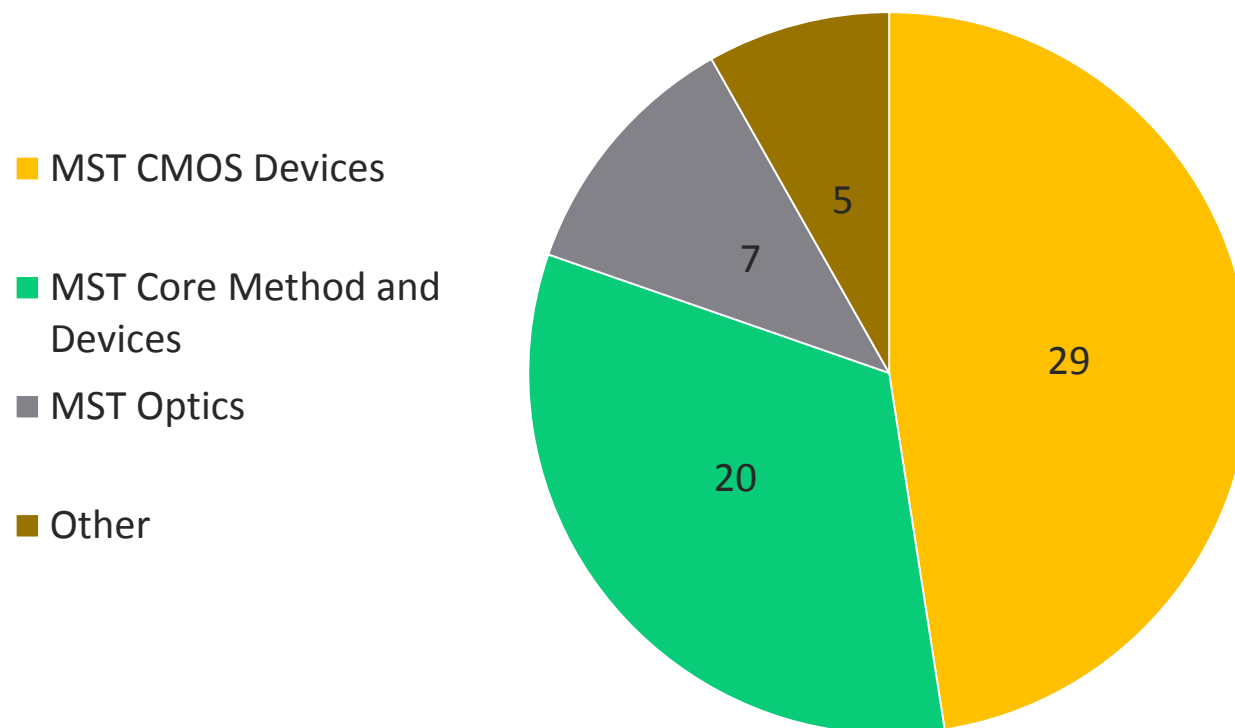
(12) <b>United States Patent</b> Mears et al.	(10) Patent No.: <b>US 9,941,359 B2</b> (45) Date of Patent: <b>April 2018</b>
(54) SEMICONDUCTOR DEVICES WITH SUPERLATTICE AND PUNCH-THROUGH STOP (PTS) LAYERS AT DIFFERENT DEPTHS AND RELATED METHODS	
(71) Applicant: <b>Atomera, Incorporated</b> , Los Gatos, CA (US)	

(12) <b>United States Patent</b> Mears et al.	(10) Patent No.: <b>US 9,972,685 B2</b> (45) Date of Patent: <b>May 2018</b>
(54) VERTICAL SEMICONDUCTOR DEVICES INCLUDING SUPERLATTICE PUNCH THROUGH STOP LAYER AND RELATED METHODS	
(71) Applicant: <b>Atomera, Incorporated</b> , Los Gatos, CA (US)	

350nm 180nm 130nm 90nm 65nm 40nm 28nm 22nm 16nm 14nm 10nm 7nm 5nm

## *22 New US Patents Applications Filed in 2017*

### 61 Issued US Patents



- **Strong Patent Portfolio**
  - Covers core elements of MST
  - Constantly adding new patents
- **Discoverable and enforceable**
  - Infringement can be easily discovered using electron microscopy
- **International Strategy**
  - Including foreign counterparts, portfolio has over 110 granted patents

# Financials



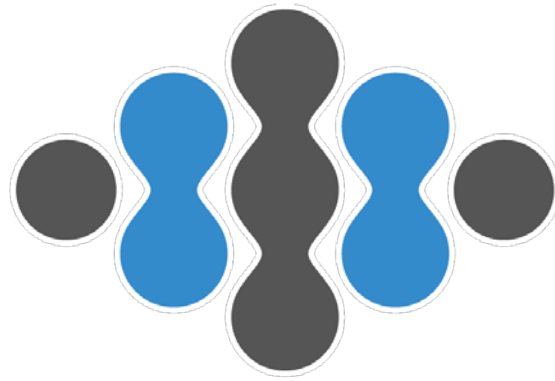
	2018 YTD		2017			
	Q2 2018	Q1 2018	Q4 2017	Q3 2017	Q2 2017	Q1 2017
<b>GAAP Results</b>						
Revenue	\$0.1M	-	\$0.1M	-	-	-
Gross Profit	(\$0.02M)	-	\$0.1M	-	-	-
Operating Expense	(\$3.2M)	(\$3.1M)	(\$2.7M)	(\$3.3M)	(\$3.7M)	(\$3.6M)
Net Loss	(\$3.2M)	(\$3.1M)	(\$2.6M)	(\$3.3M)	(\$3.6M)	(\$3.5M)
Loss Per Share	(\$0.26)	(\$0.26)	(\$0.21)	(\$0.28)	(\$0.31)	(\$0.31)
<b>Reconciliation between GAAP &amp; Non-GAAP</b>						
Net Loss (GAAP)	(\$3.2M)	(\$3.1M)	(\$2.6M)	(\$3.3M)	(\$3.6M)	(\$3.5M)
Interest Expense	-	-	-	-	-	-
Stock-Based Compensation	\$0.6M	\$0.5M	\$0.5M	\$0.9M	\$1.4M	\$1.2M
Adjusted EBITDA (Non-GAAP)*	(\$2.6M)	(\$2.6M)	(\$2.1M)	(\$2.4M)	(\$2.2M)	(\$2.4M)
Cash at June 30, 2018	\$12.3M					
Shares Outstanding at June 30, 2018	12.4M					

\* For a full reconciliation of GAAP and non-GAAP results, please see our press release issued August 8, 2018.

# Summary



- High margin, recurring revenue financial model
- Well funded with strong cash position
- Solid progress with initial customers in pipeline
- Strong technology and patent position
- Experienced management team to execute business plan



# atomera

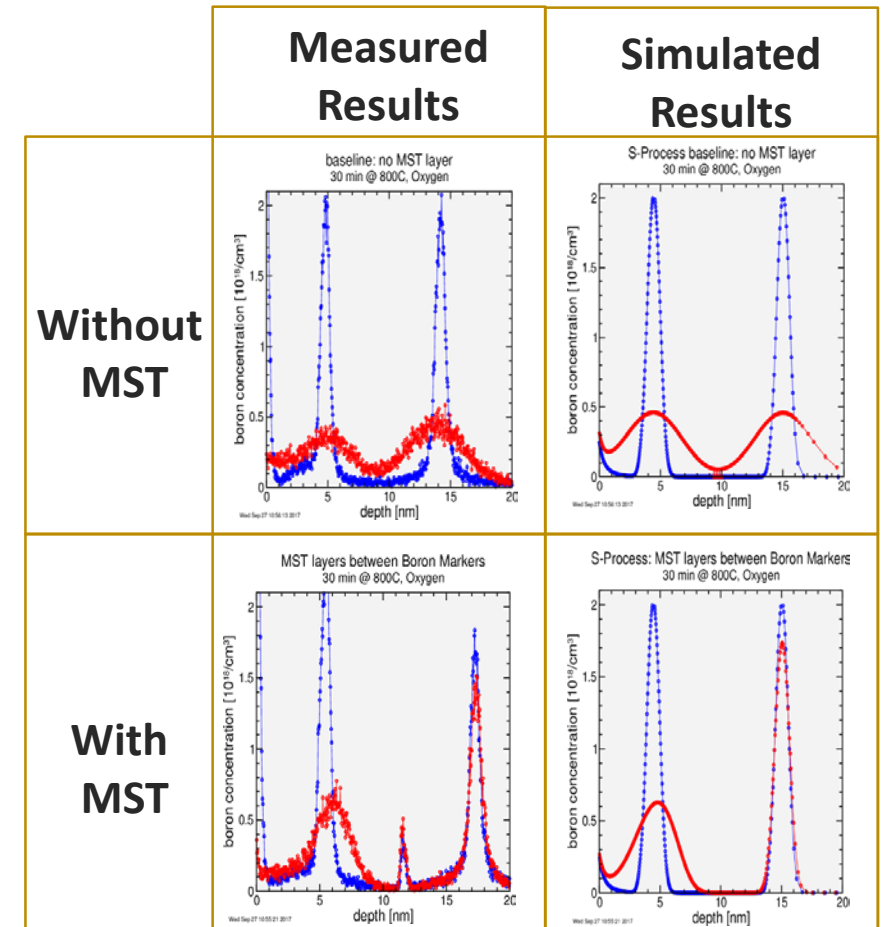
## Technology details



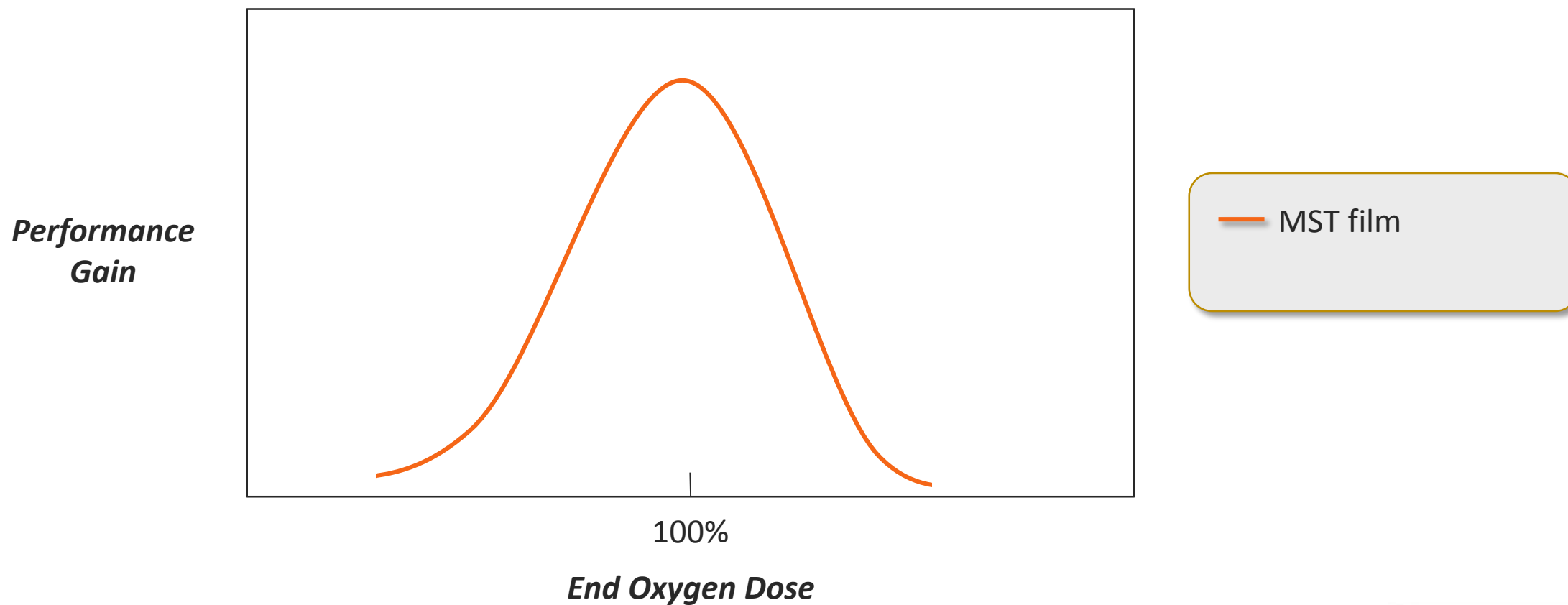
# TCAD Modelling Advantage



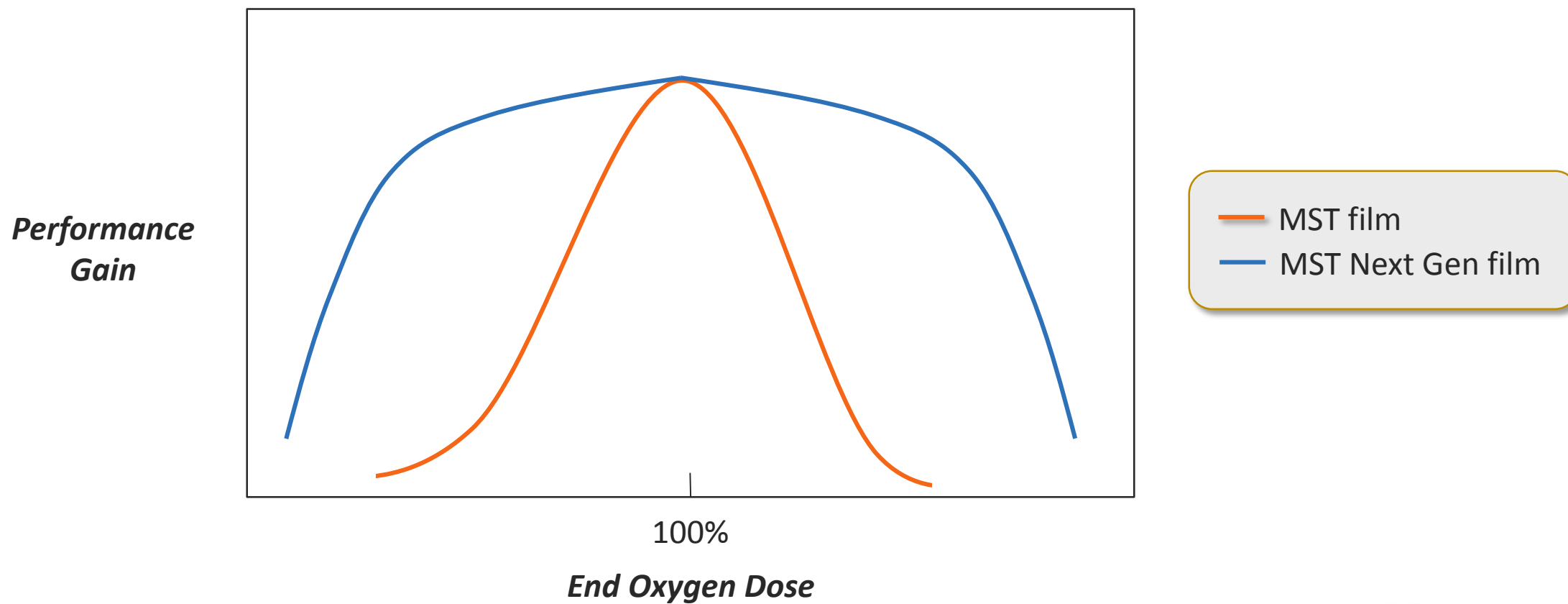
- TCAD allows customers simulate MST quickly and inexpensively
- Engages customers earlier to understand how to use MST
  - Benefits
  - Best integration techniques
- Frequently causes more ownership on customer side
- Builds early credibility and desire to experiment
  - Early license discussions
  - Horizontal buy-in at customer



# Maximizing MST Performance



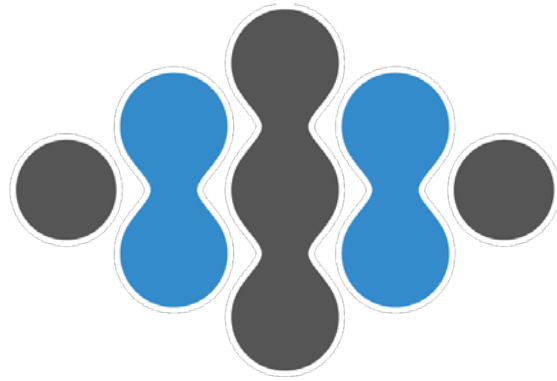
# Maximizing MST Performance



# MST and High-k/Metal gates



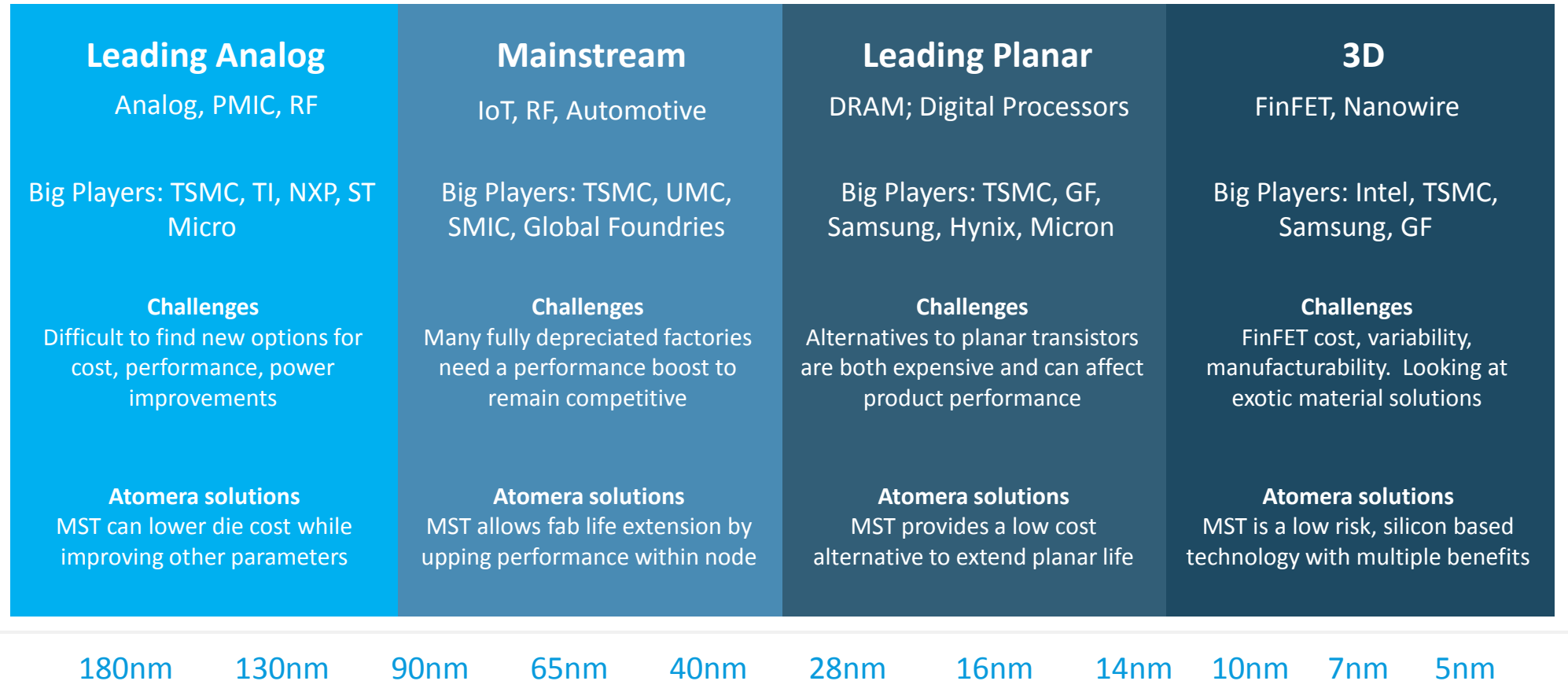
- Tests conducted on MST by the University of Notre Dame
- Results showed MST improved performance of High-k products
  - 23% mobility enhancement
  - 2.7x gate leakage reduction
- High-k/Metal gate widely used in advanced manufacturing nodes



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Backup

# Market Segment Strategy



*Now engaged with customers in all four segments*